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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,527	09/01/2000	Hideo Miyake	1614.1074	7021

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/654,527	MIYAKE ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 11-13, 15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
12/22/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 16, 2006 has been entered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 15 recites the limitation "the interface" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-8, 11-13, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Coon et al., US Patent 6,738,892 (herein after "Coon").

8. Referring to claim 1, Coon has taught a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words, wherein each of the instruction words consists of the one or more basic instructions to be executed by one or more instruction execution units (column 4, lines 48-63, column 3, lines 22-61, VLIW instructions are the claimed instruction words with individual instructions.) and delimiting information delimiting the one or more basic instructions (column 7, line 35-column 8, line 30, For a 128 bit instruction as in Table 1 and a 64 bit instruction as in table 2, all bits, except for the Memory, ALU0, ALU1 and Immediate32 bits are the claimed delimiting information.), said parallel processor comprising:

a. N instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel, where N is an integer greater than one (column 8, lines 53-65, Figure 2, at least elements 7A, 7B, 7C and 7D are the N parallel execution units.);

b. an instruction fetch unit fetching the instruction words one by one (column 7, lines 14-25, Figure 1, F0 and F1) in accordance with the instruction delimiting information to supply at least one basic instruction contained in each instruction word (column 7, line 14-column 8, line 30, The VLIW instructions are fetched in accordance with delimiting information that delimits 64 or 128 bit instructions. The instructions are fetched so that they can be supplied to the individual pipelines in Figure 2.); and

c. an instruction issue unit issuing N instruction pairs in response to the at least one basic instruction supplied from said instruction fetch unit, the N instruction pairs being supplied to N respective instruction execution units for execution of the one or more basic instructions contained in the given instruction word (Figure 2, at least elements 13, F1, RF, XA, XB, M0, M1, DE, and EX comprise the claimed instruction issue unit issuing N instruction pairs. A pair is an instruction and an enable bit.),

d. wherein each of the N instruction pairs supplied to a corresponding N instruction execution unit includes a basic instruction and a single effective bit controlling whether the basic instruction is to be executed by the corresponding instruction execution unit (column 10, lines 55-62, Figure 2, the enable bit in element 13 is the claimed single effective bit, column 4, line 63-column 5, line 12).

9. Referring to claim 2, Coon has taught the parallel processor as claimed in claim 1, as described above, and wherein the N instruction execution units all have the same structure (Figure 2, column 7, line 35-column 8, line 30, Figure 1, element 7, column 6, lines 51-59, When there are two ALU instructions in the VLIW, then the two execution units, ALU1 and ALU0, have the same structure.).

10. Referring to claim 3, Coon has taught the parallel processor as claimed in claim 1, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (figure 2, column 7, line 35-column 8, line 30, Elements 7C and 7D are different from 7A and 7B, Figure 1, element 7, column 6, lines 51-59); and

b. the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the execution units, and then supplies the rearranged basic instructions to the instruction issue unit (column 8, lines 53-60, Figure 2, The VLIW instruction is rearranged by separating out the individual instructions and sending them to their respective pipeline.).

11. Referring to claim 4, Coon has taught the parallel processor as claimed in claim 1, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (figure 2, column 7, line 35-column 8, line 30, Elements 7C and 7D are different from 7A and 7B, Figure 1, element 7, column 6, lines 51-59); and

b. the instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (column 8, lines 53-60, Figure 2, The VLIW instruction is rearranged by separating out the individual instructions and sending them to their respective pipeline.).

12. Referring to claim 5, Coon has taught the parallel processor as claimed in claim 1, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (figure 2, column 7, line 35-column 8, line 30, Elements 7C and 7D are different from 7A and 7B, Figure 1, element 7, column 6, lines 51-59);

b. the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit (column 8, lines 53-60, Figure 2, The VLIW instruction is rearranged by separating out the individual instructions and sending them to their respective pipeline.); and

c. the instruction issue unit further rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (column 8, lines 53-60, Figure 2, The VLIW instruction atoms are rearranged in the pipeline, such that they advance from stage-to-stage in accordance with their respective pipeline, which contains an appropriate execution unit. The instructions are ultimately supplied to execution unit elements 7A, 7B, 7C and 7D.).

13. Referring to claim 6, Coon has taught the parallel processor as claimed in claim 3, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (figure 2, column 7, line 35-column 8, line 30, Elements 7C and 7D are different from 7A and 7B, Figure 1, element 7, column 6, lines 51-59); and

b. the instruction fetch unit fetches an instruction word that contains basic instructions arranged in advance in accordance with the arrangement of the instruction execution units (column 7, line 35-column 8, line 30, Tables 1 and 2, VLIW instructions are arranged in advance in accordance with the available execution units in the processor.).

14. Referring to claim 7, Coon has taught the parallel processor as claimed in claim 1, as described above, and wherein, depending on the type of a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of the basic instruction being currently executed is completed (column 7, line 14-column 8, line 65 Instruction atoms in the VLIW molecule are issued and executed in parallel in a pipelined system. Pipelined systems contain several basic instructions are executing in the pipeline at any given time such that many basic instructions are issued while several basic instructions have not yet completed.).

15. Referring to claim 8, Coon has taught the parallel processor as claimed in claim 7, as described above, and wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues the supplied basic instruction before the execution of the basic instruction being currently executed is completed (Column 7, lines 3-34, column 8, lines 46-65, Only one of the above mentioned items needs to be met as they are referred to in the alternative. Coon has at least taught not sharing resources. Instructions are issued into the earlier pipeline stages while basic instructions are executing in the execution units later in the pipeline, elements 7, 7A, 7B, 7C and 7D. A basic instruction currently executing in elements 7, 7A, 7B, 7C and 7D does not share the pipeline stage of an instruction in the earlier stages and therefore does not share resources. This is the description and benefit of a pipelined system. A pipelined system executes many instructions at once.).

16. Referring to claim 11, Coon has taught a parallel processor as claimed in claim 1, as described above, and wherein a first instruction word format is converted into a second instruction word format, the first instruction word format indicating a first arrangement of

instruction words from the instruction fetch unit, and the second instruction word format indicating a second arrangement of instruction words which corresponds to the instruction execution units (Column 7, lines 3-34, column 8, lines 46-65, column 10, lines 55-62, VLIW instructions, or molecules, are fetched from memory. The molecules are the first instruction word format. The individual instructions in the molecule, or atoms, are issued to respective execution units along with enable, or effective, bits. The atoms and the effective bits in their corresponding pipelines comprise the second instruction word format.).

17. Referring to claim 12, Coon has taught a parallel processor as claimed in claim 1, as described above and further comprising a conversion unit, wherein the conversion unit converts a first instruction word format into a second instruction word format on the basis of the effective bit, corresponding to the instruction execution units, indicating whether the corresponding instruction execution unit is available (Column 7, lines 3-34, column 8, lines 46-65, column 10, lines 55-62, The effective bit indicates whether the execution unit is available, or qualified to execute the instruction. When the effective bit is set to zero then the execution unit is not qualified to execute the instruction as the instruction should not be executed. The instruction should instead be masked. VLIW instructions, or molecules, are fetched from memory. The molecules are the first instruction word format. The individual instructions in the molecule, or atoms, are issued to respective execution units along with enable, or effective, bits. The atoms and the effective bits comprise the second instruction word format. The first instruction word format is converted to a second instruction word format when the instructions and enable bits are issued to the pipelines.).

18. Referring to claim 13, Coon has taught a parallel processor as claimed in claim 12, as described above, and wherein the first instruction word format indicates a first arrangement of instruction words from the instruction fetch unit, and the second instruction word format

indicates a second arrangement of instruction words which corresponds to the instruction execution units (Column 7, lines 3-34, column 8, lines 46-65, column 10, lines 55-62, A VLIW instruction molecule, or first instruction word format, is fetched from memory and converted to instruction atoms and enable, or effective, bits that are each arranged into their respective pipeline corresponding to their respective execution unit.).

19. Referring to claim 15, Coon has taught a parallel processor as claimed in claim 1, as described above, and wherein the instruction issue unit issues the basic instructions to the corresponding instruction execution unit based on the interface (Column 7, lines 3-34, column 8, lines 46-65, column 10, lines 55-62, The effective bits/enable bits are interpreted to be set by the interface. The values set in the effective bits determine which instructions are executed and which instructions are masked. Masked instructions are not issued for execution within the execution units.).

20. Referring to claim 16, Coon has taught a parallel processor performing parallel processing of at least one basic instruction contained in each of a plurality of instruction words, each of the instruction words consisting of the at least one basic instruction to be executed by at least one instruction execution unit (column 4, lines 48-63, column 3, lines 22-61, VLIW instructions are the claimed instruction words with individual instructions.) and delimiting information only delimiting the at least one basic instruction (column 7, line 35-column 8, line 30, For a 128 bit instruction as in Table 1 and a 64 bit instruction as in table 2, all bits, except for the Memory, ALU0, ALU1 and Immediate32 bits, are the claimed delimiting information.), said parallel processor comprising:

a. instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (column 8, lines 53-65, Figure 2, at least elements 7A, 7B, 7C and 7D are the claimed parallel execution units.);

b. an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information (column 7, line 14-column 8, line 30, The VLIW instruction words are fetched in accordance with delimiting information that delimits 64 or 128 bit instructions. The instructions are fetched so that they can be supplied to the individual pipelines in Figure 2.); and

c. an interface setting effective bits each corresponding to one of the instruction execution units and indicating a corresponding instruction execution unit for each basic instruction to be executed from each instruction word (column 10, lines 55-62, Figure 2, the enable bits in element 13 are the claimed effective bits, when the effective bit is set the corresponding execution unit executes the instruction, and when the effective bit is not set then the corresponding execution unit does not execute the instruction, column 4, line 63-column 5, line 12), checking codes of the at least one basic instruction to identify the at least one basic instruction and determine the corresponding instruction execution unit for each basic instruction (column 7, lines 14-25, column 7, lines 63-67, column 8, lines 52-65, The instructions codes are fetched, decoded and routed to the appropriate pipeline (including an associated execution unit.) based on the instruction opcode type, e.g. ALU, memory, or floating point.).

Response to Arguments

21. Applicant's arguments with respect to claims 1-8, 11-13, 15 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Pechanek et al., US Patent 6,467,036, has taught disabling sub-instruction words in a VLIW instruction.

b. Pechanek et al., US Patent 6,151,668, has taught disabling sub-instruction words in a VLIW instruction.

c. Blaner et al., US Patent 5,214,763, has taught an instruction compounding sysystem.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

tlm

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